UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,897	03/30/2004	Kimmo Mylly	915-005.098	5044

4955 7590 04/17/2007	EXAMINER
WARE FRESSOLA VAN DER SLUYS & ADOLPHSON, LLP	SONG, JASMINE

BRADFORD GREEN, BUILDING 5	ART UNIT	PAPER NUMBER
755 MAIN STREET, P O BOX 224 MONROE, CT 06468	2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>02 February 2007</u>.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-22* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

Detailed Action

1.   This office action is in response to Amendment filed 02/02/2007. All rejections

and objections not explicitly repeated below are withdrawn.

Specification

2.   The lengthy specification has not been checked to the extent necessary to

determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the

specification.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as
> set forth in section 102 of this title, if the differences between the subject matter sought to be
> patented and the prior art are such that the subject matter as a whole would have been obvious
> at the time the invention was made to a person having ordinary skill in the art to which said
> subject matter pertains. Patentability shall not be negatived by the manner in which the invention
> was made.

4.   Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ootani et al., US patent 6,959,365 B2, in view of Pline., US 2004/0098545 A1.

        Regarding claim 1, Ootani teaches a method for performing a processing

function (it is taught as one of a series of processing such as erase/write or rewrite) of a

memory in a block memory comprising memory cells where data can be stored (Fig.1

and Fig.2), and a connection bus comprising at least a ready/busy line (Fig.1, RYIBY),

which can be set at least to a ready status and to a busy status (col.4, lines 1-8 and

col.5, lines 35-41), said method comprising setting the status of said ready/busy line to

said busy status in a beginning of the processing function (col.5,lines 35-37), indicating

an end of processing function by setting said ready/busy line to said ready status

(col.5,lines 37-38), and changing the status of said ready/busy line back to said busy

status if a rewrite command is detected (col.5, lines 43-47). Ootani does not teach

performing detection of processing errors and changing the status of said ready/busy

line back to said busy status if a processing error is detected. However, Pline teaches

performing detection of processing errors (section 0064, last seven lines) and changing

the status of said ready/busy line back to said busy status if a processing error is

detected (section 0034, lines 11 to last line of this paragraph). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to utilize the

teachings of Pline into Ootani's system such as performing detection of processing

errors and changing the status of said ready/busy line back to said busy status if a

processing error is detected because the fast serial transfer circuit preferably comprises

error detection and correction circuitry, synchronization detecting circuitry, and eight bit

to ten bit encoder, and a ten bit to eight bit decoder to facilitate encoding of clock and

data, to allow separation of clock and data, and to facilitate decoding of data (see Pline,

section 0032, last nine lines), therefore, providing a higher performance, faster data

transfer rate of memory system.

Accordingly, one of ordinary skill in the art would have recognized this and

concluded that they are from the same field of endeavor. This would have motivated

one of ordinary skill in the art to implement the above combination for the advantages

set forth above.

Regarding claims 11,19-20 and 22, Ootani teaches a system, which comprises

an electronic device comprising a block memory comprising memory cells for storing

data (Fig.1 and Fig.2), and a connection bus comprising at least a ready/busy line, and

at least a ready status and a busy status are defined for said ready/busy line (Fig.1,

RYIBY; col.4, lines 1-8 and col.5, lines 35-41), and which block memory comprises

means for changing the status of said ready/busy line to said busy status in the

beginning of the processing function of the block memory (col.5,lines 35-37), and

means for indicating the end of processing function by setting said ready/busy line to

said ready status (col.5,lines 37-38), the system further comprising means for changing

the status of said ready/busy line back to said busy status if a rewrite command is

detected (col.5, lines 43-47). Ootani does not teach a comparator for detecting

processing errors and changing the status of said ready/busy line back to said busy

status after a processing error is detected. However, Pline teaches a comparator for

detecting processing errors (section 0064, last seven lines) and changing the status of

said ready/busy line back to said busy status if a processing error is detected (section

0034, lines 11 to last line of this paragraph). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to utilize the teachings of

Pline into Ootani's system such as performing detection of processing errors and

changing the status of said ready/busy line back to said busy status if a processing error

is detected because the fast serial transfer circuit preferably comprises error detection

and correction circuitry, synchronization detecting circuitry, and eight bit to ten bit

encoder, and a ten bit to eight bit decoder to facilitate encoding of clock and data, to

allow separation of clock and data, and to facilitate decoding of data (see Pline, section

0032, last nine lines), therefore, providing a higher performance, faster data transfer

rate of memory system.

Accordingly, one of ordinary skill in the art would have recognized this and

concluded that they are from the same field of endeavor. This would have motivated

one of ordinary skill in the art to implement the above combination for the advantages

set forth above.

Regarding claim 2, Ootani teaches erasing the block memory is used as said

processing function, the method comprising performing a comparison of an erased

memory cell with the data meant for the status of the erased memory cell in connection

with erasing, in order to detect erasing errors, and if an erasing error is detected in the

comparison, changing the status of said ready/busy line back to said busy status (col.4,

lines 1-8, it is taught as erase command has been accepted in the flash memory).

Regarding claim 3, Ootani teaches storing data to the block memory is used as

said processing function, the method comprising performing a comparison of stored

data with data meant to be stored in connection with storing the data, in order to detect storing errors, and if a storing error is detected in the comparison, changing the status of said ready/busy line back to said busy status (it is taught as write command has been accepted in the flash memory, col.4, lines 1-8).

Regarding claim 4, Ootani teaches copying data in the block memory from one location to some other location is used as said processing function, the method comprising performing a comparison of copied data with data meant to be copied in connection with copying the data, in order to detect copying errors, and if a copying error is detected in the comparison, changing the status of said ready/busy line back to said busy status (Ootani does not specifically teach copying operation, Ootani teaches erase, write or mode transition activities issued to the flash memory module form the CPU are all referred to "rewrite", therefore, copy operation can be considered as rewrite, col.6, lines 17-21 and col.5, lines 42-46).

Regarding claim 5, Ootani teaches reading data from the block memory is used as said processing function, the method comprising performing examining status of a memory cell being read in connection with reading data, and if a memory cell error is detected in the examination, changing the status of said ready/busy line back to said busy status (col.3, lines 58-64).

Regarding claim 6, Ootani teaches comprising starting the processing function by sending a command to the block memory (col.4, lines 51-56), and setting the status of said ready/busy line to the busy status in a stage when a function according to the command is started in the block memory (col.5, lines 35-37).

Regarding claim 7, Ootani teaches the block memory (memory block 14) is divided into blocks and each block is divided into pages, the method comprising transmitting data to the block memory page by page (Fig.3).

Regarding claims 8 and 17, Ootani teaches comprising performing erasing of at least one block, and setting a previously determined status as the status of all the memory cells of said at least one block (col.7, lines 27-35).

Regarding claim 9, Ootani teaches comprising examining the status of said ready/busy line, and performing re-examination of the status of the ready/busy line when it changes from the busy status to the ready status (col.8, lines 51-57).

Regarding claims 10 and 18, Ootani teaches the connection bus comprises a data bus comprising at least one data line, the method comprising using the data line of said data bus as a ready/busy line (Fig.1).

Regarding claims 12 and 21, Ootani teaches the processing function is one of

the following: emptying the memory cells, storing data in memory cells, copying data

between memory cells, reading the data stored in the memory cells (col.4, lines1-8).

Regarding claim 13, Ootani teaches comprising a processor (Fig.1), and a first

connection bus between the processor and the block memory, and means for starting

the processing function by sending a command to the block memory (Fig.1), and means

for setting the status of said ready/busy line to the busy status when the function

according to the command has been started in the block memory (col.5, lines 35-37).

Regarding claim 14, Ootani teaches comprising means for creating an interrupt

in the processor (col.8, lines 46-49) when the status of the ready/busy line changes

from the busy status to the ready status, and the processor comprising means for

examining the status of the ready/busy line in connection with handling the interrupt

(col.8, lines 41-57).

Regarding claim 15, Ootani teaches comprising a processor(Fig.1), a memory

controller, a first connection bus between the processor and the memory controller

(Fig.1), and a second connection bus between the memory controller and the block

memory (Fig.1), in which case the commands are arranged to be sent from the

processor to the memory controller, as well as from the memory controller to the block

memory (Fig.1), the system comprising means for starting storing of the data by sending

a command to the block memory(Fig.1), and means for setting the status of said

ready/busy line to the busy status when the function according to the command has

been started in the block memory (col.5, lines 35-37).

Regarding claim 16, Ootani teaches comprising means for creating an interrupt in

the memory controller (col.8, lines 46-49) when the status of the ready/busy line

changes from the busy status to the ready status, wherein the memory controller

comprises means for examining the status of the ready/busy line in connection with

handling the interrupt, and means for forming an interrupt to the processor if the

ready/busy line is in the busy status (col.8, lines 41-57).

Response to Arguments

5.   Applicant's arguments with respect to claims 1-22 have been considered but are

moot in view of the new ground(s) of rejection.

6.   When responding to the office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show

how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

7.   When responding to the office action, Applicants are advised to provide the

examiner with the line numbers and page numbers in the application and/or references

cited to assist examiner to locate the appropriate paragraphs.

8.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Jasmine Song whose telephone number is 571-272-

4213. The examiner can normally be reached on 7:30-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jasmine Song

Patent Examiner

April 13, 2007